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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/800,630	03/16/2004	Kazuhiro Tashiro	042236	9692

38834 7590 09/14/2007

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EXAMINER	
HUYNH, ANDY	

ART UNIT	PAPER NUMBER
2818	

MAIL DATE	DELIVERY MODE
09/14/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/800,630	TASHIRO ET AL.	
	Examiner	Art Unit	
	Andy Huynh	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 August 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7-10 and 12-25* is/are pending in the application.

4a) Of the above claim(s) *1-4,21 and 22* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5,7-10,12-20,24 and 25* is/are rejected.

7)☒ Claim(s) *23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination (RCE) under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission and Amendment filed on August 20, 2007 has been entered.

In light of the Amendment filed with RCE on August 20, 2007, claims **6 and 11** have been canceled. Claims **1-4, 21, and 22** have been withdrawn from consideration. Claims **5, 13 and 14** have been amended.

Response to Arguments

Applicant's arguments see Remarks filed August 20, 2007, with respect to the rejection(s) of claim(s) **5, 7-10, 12-20, 24 and 25** have been considered but are moot in view of the new ground(s) of rejection.

Specification

The disclosure is objected to because of the following informalities:

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The specification has been checked to the extent necessary to determine the presence of all possible minor errors. However, the applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

Claim **5** is objected to because of the following reasons.

In claim **5**, line 8, "wherein the substrate has a semiconductor chip mounted thereon" is duplicated.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims **5, 7-10, 12-20, 24 and 25** are rejected under 35 U.S.C. 103(a) as being unpatentable over JP 2001-015237 in view of US 6,828,676 to Akai.

Regarding Claim **5**, JP 2001-015237 discloses in Figs. 2 and 8 a semiconductor device protection cover 2B attached to a semiconductor device 1, comprising:

a base portion;

a first surface, said first surface being flat (Fig. 8);

a second surface having a projecting portion to be brought into contact with a substrate/housing 2A of the semiconductor device and a depressed portion not to be brought into contact with parts mounted in the semiconductor device; and

an engaging portion to engage the semiconductor device protection cover with the substrate/housing of the semiconductor device, so as to detachably attach the semiconductor device protection cover to the semiconductor device (see Fig. 2, English Abstract).

JP 2001-015237 does not explicitly disclose wherein the substrate has a semiconductor chip mounted thereon. However, Akai teaches in Figs. 1, 2, and 4 a semiconductor device having a lid 5/25 implemented on a semiconductor chip 2/22 mounted on a substrate 3/23. It would have been obvious to one having ordinary skill in the art at the time of the invention was made to incorporate a semiconductor chip mounted on a substrate, as taught by Akai into, combine and modify the JP 2001-015237 to arrive the claimed feature, the substrate has a semiconductor chip mounted thereon, since it is known in the semiconductor art that the substrate is used for mounting and supporting the semiconductor chip.

Regarding Claims **7, 8, 10 and 20**, JP 2001-015237 does not disclose the projecting portion and the base portion of the semiconductor device protection cover are formed from materials having hardness higher/lower than a surface of the semiconductor device; the projecting portion and the base portion of the semiconductor device protection cover have

conductivity; the first positioning member and the second positioning member are formed by recognition marks. It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form the projecting portion and the base portion of the semiconductor device protection cover from materials having hardness higher/lower than a surface of the semiconductor device, and the projecting portion and the base portion of the semiconductor device protection cover have conductivity, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416. Also, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to form the first positioning member and the second positioning member by recognition marks in order to align the first positioning member and the second positioning member.

Regarding Claims **9 and 13**, JP 2001-015237 discloses in Figs. 2 and 8 a semiconductor device protection cover 2B attached to a semiconductor device 1, comprising:

a base portion;

a first surface, said first surface being flat (Fig. 8); and

a second surface to be brought into contact with a substrate/housing 2A of and parts mounted in the semiconductor device, said second surface being formed from an elastic material (par. [0009]),

wherein the semiconductor device protection cover has a structure to engage with the semiconductor device so as to be detachably attached to the semiconductor device (see Fig. 2, English Abstract).

JP 2001-015237 does not explicitly disclose wherein the substrate has a semiconductor chip mounted thereon. However, Akai teaches in Figs. 1, 2, and 4 a semiconductor device having a lid 5/25 implemented on a semiconductor chip 2/22 mounted on a substrate 3/23. It would have been obvious to one having ordinary skill in the art at the time of the invention was made to incorporate a semiconductor chip mounted on a substrate, as taught by Akai into, combine and modify the JP 2001-015237 to arrive the claimed feature, the substrate has a semiconductor chip mounted thereon, since it is known in the semiconductor art that the substrate is used for mounting and supporting the semiconductor chip.

Regarding Claims **12, 24 and 25**, JP 2001-015237 discloses in Fig. 2 the base portion has a predetermined shape irrespective of an outer shape of the semiconductor device; the depressed portion forming an opening penetrating through the base portion; and the depressed portion forming a plurality of openings penetrating through the base portion and a plurality of ribs between the openings.

Regarding Claim **14**, JP 2001-015237 discloses in Figs. 2 and 8 a semiconductor device unit, comprising:

a semiconductor device 1; and

a semiconductor device protection cover 2B,

wherein the semiconductor device protection cover comprises:

a base portion;

a first surface, said first surface being flat (Fig. 8); and

a second surface having a projecting portion to be brought into contact with a

substrate/housing 2A of the semiconductor device and a depressed portion not to be brought into

contact with parts mounted in the semiconductor device,

wherein the semiconductor device protection cover has a structure to engage with the semiconductor device so as to be detachably attached to the semiconductor device (see Fig. 2, English Abstract).

JP 2001-015237 does not explicitly disclose wherein the substrate has a semiconductor chip mounted thereon. However, Akai teaches in Figs. 1, 2, and 4 a semiconductor device having a lid 5/25 implemented on a semiconductor chip 2/22 mounted on a substrate 3/23. It would have been obvious to one having ordinary skill in the art at the time of the invention was made to incorporate a semiconductor chip mounted on a substrate, as taught by Akai into, combine and modify the JP 2001-015237 to arrive the claimed feature, the substrate has a semiconductor chip mounted thereon, since it is known in the semiconductor art that the substrate is used for mounting and supporting the semiconductor chip.

Regarding Claims **15-17**, JP 2001-015237 discloses in Fig. 2 the semiconductor device has a first positioning member; and the semiconductor device protection cover has a second positioning member, the semiconductor device and the semiconductor device protection cover being set in position when the first positioning member and the second positioning member are engaged with each other; the first positioning member is a projection; and the second positioning member is a recess engagable with the projection; wherein an inclined surface 2C is formed on the projection for guiding insertion of the projection into the recess.

Regarding Claims **18 and 19**, JP 2001-015237 discloses in Fig. 2 the first positioning member is a peripheral part of the semiconductor device; and the second positioning member is a wall engagable with the peripheral part; wherein an inclined surface 2C is formed on the second positioning member for guiding the first positioning member to engage with the second positioning member.

Allowable Subject Matter

Claim **23** is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations.

Conclusion

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andy Huynh, (571) 272-1781. The examiner can normally be reached on Monday-Friday from 6:30 AM to 3:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Loke can be reached on (571)

272-1657. The Fax number for the organization where this application or proceeding is assigned is (571) 273-8300.

Any inquiry of a general nature or relating to the -status of this application or proceeding should be directed to the receptionist whose phone number is (703) 308-0956.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ah

Andy Huynh
Primary Examiner